IN THE CLAIMS

1. - 11. (Cancelled)

12. (Original) A method of electrically accessing a plurality of integrated circuits, each integrated circuit having a plurality of terminals, the method comprising:

providing a wafer having a first and a second major surface, the plurality of integrated circuits disposed on a first major surface thereof, each of the plurality of integrated circuits having a plurality of terminals, and the plurality of integrated circuits disposed over at least a portion of the first major surface;

providing a full wafer contacter having a first major surface and a second major surface, a first plurality of contact terminals disposed on the first major surface of the full wafer contacter in a pattern that corresponds to the terminal layout of the plurality of integrated circuits; and

removably attaching the full wafer contacter to the wafer such that the first major surface of the wafer and the first major surface of the full wafer contacter are facing each other, and such that at least a portion of the terminals of the integrated circuits are in electrical contact with the first plurality of contact terminals;

wherein each of the first plurality of contact terminals is electrically coupled to a corresponding one of a second plurality of contact terminals disposed on the second major surface of the full wafer contacter.

13. (Original) The method of claim 12, wherein removably attaching comprises vacuum attaching.

14. (Original) The method of claim 12, wherein removably attaching comprises producing a low pressure zone between the full wafer contacter and the wafer.

15. (Original) The method of claim 14, wherein removably attaching comprises, in an atmosphere containing one or more gases, placing the full wafer contacter over the wafer, and evacuating at least a portion of the one or more gases disposed between the full wafer contacter and the wafer.

16. (Original) The method of claim 12, wherein the integrated circuit terminals comprise bonding pads.

17. (Original) The method of claim 12, wherein the integrated circuit terminals comprise solder bumps.

18. (Original) The method of claim 12, further comprising aligning the full wafer contacter to the wafer such that the terminals of the integrated circuits and the terminals disposed on the first major surface of the full wafer contacter will be in electrical contact when the full wafer contacter is removably attached to the wafer.

19. (Original) The method of claim 12, wherein a first portion of the plurality of integrated circuits has a first terminal layout pattern, and a second portion of the plurality of integrated circuits has a second terminal layout pattern, and the first and second terminal layout patterns are different.

20. (Original) The method of claim 19, wherein each of the first portion of the plurality of integrated circuits has a first die size, and each of the second portion of the plurality of integrated circuits has a second die size, and the first and second die sizes are different.

21. (New) The method of Claim 12, wherein the wafer has a first area, the full wafer contacter has a second area, and the first area is greater than the second area.

22. (New) The method of Claim 12, further comprising seating a sealing ring in a groove of the full wafer contacter prior to removably attaching the full wafer contacter to the wafer.

23. (New) The method of Claim 12, wherein the full wafer contacter is thinner than the wafer.

24. (New) The method of Claim 12, further comprising introducing an inert gas between the full wafer contacter and the wafer.